8Mbit to 256MBit HyperMemory®
SRAM and FIFO

Features

- Super high-speed Static-Memory
- Can be configured as a standalone FIFO
- Supports multiple IO Standards (HSTL, SSTL, LVCMOS/ LVTTL)
- Access time as low as 3ns in Asynchronous mode
- As high as 500MHz clock speed in pipe-lined Sync mode (1-Cycle), 800MHz in 2-Cycle pipe-lined Sync mode and 1GHz in 3-Cycle pipe-lined Sync Mode
- FIFO Mode operates at max 1GHz Clock
- User-Selectable x8, x16 and x32 configuration
- Low-cost alternative to DRAM memory chips
- Easy to use, basic SRAM interface (Data, Address, Clock/Strobe) with no special requirements
- Configurable as 8Bit, 16Bit and 32Bit words with Byte-Select
- Very low static and dynamic power draw
- Core-Voltage Vdd at 1.2V, IO Vdd up to 3.3V LVCMOS, 1.5V for HSTL/SSTL
- Address pins convert to Data-Input in FIFO Mode
- Available in LQFP-144 package

Applications

- Low-Cost FPGA external memory (BlockRAM equivalent interface, requiring no memory controller)
- Low-Cost MCU external memory, simplifying optimization due to immediate random access
- Modems, Routers and Switches, replacing DRAMs with Low-Cost SRAMs
- Military/Defense (superior EMI resistance compared to capacitor-based DRAM memory)
- High-Speed networking and Fiber-Transmission (used as FIFO before/after SerDes)
- Low-Cost easy-to-use alternative to DRAM in industrial applications
- Disk-Drive cache
- Digital Camera and Image-Processing (General Memory, Frame-Buffers, etc.)
- GPS Navigators
- Portable Gaming Consoles
- Oscilloscopes and High-Speed Lab Instruments

Configurations

SS32HM008-LQ144: 8Mbit
SS32HM064-LQ144: 64Mbit
SS32HM128-LQ144: 128Mbit
SS32HM256-LQ144: 256Mbit

Introduction

HyperMemory® Series is a family of next generation Synchronous and Asynchronous High-Speed Low-Cost Static RAM (SRAM) and FIFO, designed to compete with the DRAM industry in the embedded market.

The simple interface, along with no requirement of Memory-Controller, allows this SRAM to be used by Low-Cost FPGAs and Microcontroller chips, improving overall performance, design simplicity, time-to-market and Bill-Of-Material (BOM).

In Asynchronous mode, access to any region in the chip takes only 2ns (HSTL/SSTL) or 4.5ns (LVCMOS/LVTTL) for both read and write operations.

Once in Synchronous mode, the device accepts clocks as high as 1GHz, operating in a pipelined manner with only 3-Cycles Latency (one cycle to push the address and two wait cycles). This allows a bandwidth in excess of 4GBytes/s (in x32 mode) with no handshake overhead, eliminating the need for fetch-prediction, which in turn dramatically improves design simplicity, reduces gate-count (in FPGAs) and simplifies timing optimization.

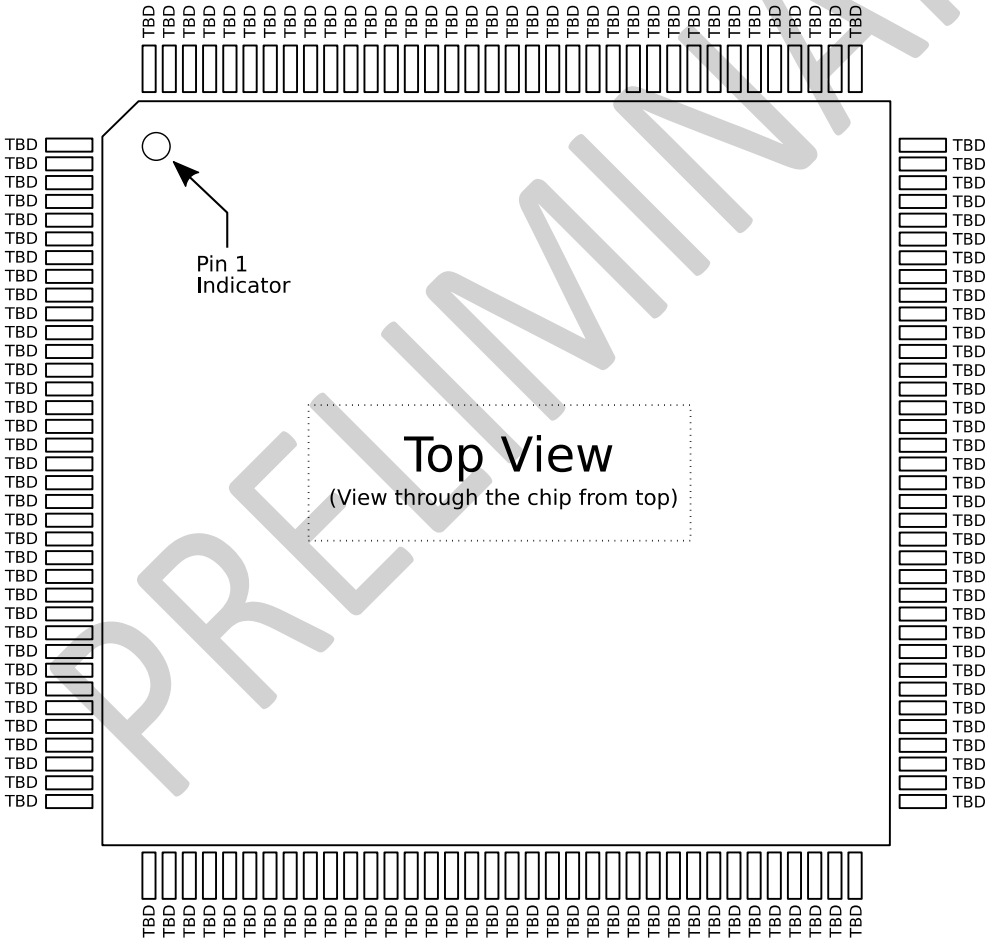
The device also supports FIFO mode, in which the unit can accept data at clock rates in excess of 1GHz. This can be very useful as frame-buffer, XFPD/Fiber modules, crossing high-speed clock-domains, Direct Digital Synthesis, etc.

Supporting LVCMOS and HSTL/SSTL IO standard allows easy communication with MCU, DSP and FPGAs (random access latency depends on the type of IO used, with HSTL/SSTL being faster).

Product Selection Guide

MODEL	CAPACITY	MAX. DEPTH	MAX. WIDTH	MAX SYNC FREQ	MIN ASYNC LATENCY	PACKAGE
SS32HM008	8MBit	256K x 32	1M x 8	1.0 GHz	3.0ns – HSTL/SSTL 4.5ns – LVCMOS	LQFP-144
SS32HM064	64MBit	1,024K x 32	8M x 8	1.0 GHz	3.0ns – HSTL/SSTL 4.5ns – LVCMOS	LQFP-144
SS32HM128	128MBit	2,048K x 32	16M x 8	1.0 GHz	3.0ns – HSTL/SSTL 4.5ns – LVCMOS	LQFP-144
SS32HM256	256MBit	4,096K x 32	32M x 8	1.0 GHz	3.0ns – HSTL/SSTL 4.5ns – LVCMOS	LQFP-144

Package Drawing and Pinout Overview



LQFP-144 Package

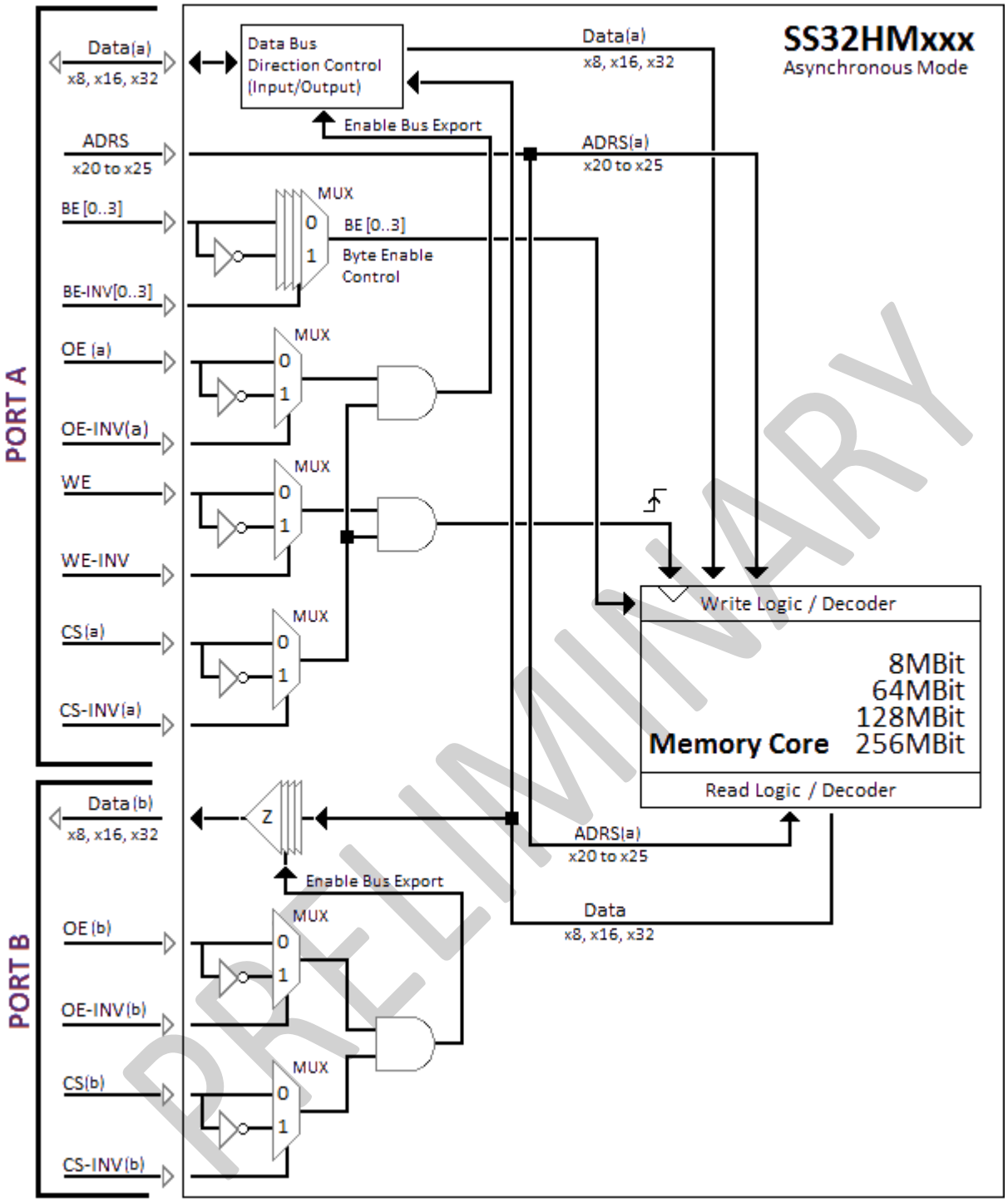
All models come in this standard package format,
with the exception of Military Grade Chips.

Pinout description

Name	IO Type	Pin Location(s)	Description
		PORT A	
Data(a) [0..31]	Input/Output	TBD	**Data Port.** Both input and output (selected by OE). In FIFO mode, this port will be input only and is used to feed data into the FIFO.
ADRS[0..24]	Input	TBD	**Address port**. Data will be written to / read from this address. It is disabled in FIFO mode
BE[0..3]	Input	TBD	**Byte-Enable**. The MSB represents Bits 24 to 31 of the data. If set, this byte will be written to memory.
BE-INV[0..3]	Input	TBD	**Byte-Enable Inverter**. If set to one, BE bits will become inverted logic (1 = Inactive, 0 = Active). This can be used comptability pursposes.
OE(a)	Input	TBD	**Output Enable**. Once set, the Data(a) port will be switched to output-mode. When reset, Data(a) port will be in input mode (and High-Impedance)
OE-INV(a)	Input	TBD	**Output Enable Inverter**. (OE becomes OE#)
WE(a)	Input	TBD	**Write-Enable**. In Asychnronous mode, a rising edge on this pin will write data to the SRAM (or FIFO if selected). In synchronous mode, if set, upon each clock rising edge (or negative edge if clock-invert was selected, a write will occur).
WE-INV(a)	Input	TBD	**Write-Enable-Inverter**. If set, it will convert WE to WE#.
RD(a)	Input	TBD	**Read-Enable**. In asynchronous mode, when set, the SRAM will provide data located at the desired address (after a fixed latency). In synchronous mode, this needs to be set before clock rising edge to enable a read. In FIFO mode, this pin is NOT USED and must be connected to ground in this case.
RD-INV(a)	Input	TBD	**Read-Enable-Inverter.** If set, the RD will be converted to RD#.
CS(a)	Input	TBD	**Chip Select (for Port A).** When set, Port-A will respond to commands, and Data-port would activate when requested by OE. When reset, the chip will not respond to commands, and Data(a) and 'FULL' pin will remain High-Z.
CS-INV(a)	Input	TBD	**Chip-Select-Inverter (for port A).** This converts CS(a) to CS(a)#.
CLOCK(a)	Input	TBD	**Sync. Clock.** Not used when chip is in Asynchronous mode, but functions as synchronous clock in both Sync FIFO and Sync SRAM modes. Connect to ground when operating in Asynchronous Mode.
CLOCK-INV(a)	Input	TBD	**Sync. Clock Inverter.** Once set, in synchronous mode, the chip will respond to falling edges of the clock, instead of rising edge. Not used in Asynchronous mode, and needs to be connected to ground in this scenario.
FUL L	Output	TBD	**FIFO Full Indicator.** When set, it indicates that FIFO is full and cannot accept more data. Must be left unconnected when the chip is in SRAM mode.
FULL-INV	Input	TBD	**FIFO Full Indicator Inverter.** Inverts the 'FULL ' pin. Once set, FULL pin will be inverted (i.e. 0 = FIFO FULL, 1 = FIFO NOT FULL)
		PORT B	
Data(b)[0..31]	Output	TBD	**Data Port.** In SRAM mode, when OE(b) is set, this port will reflect the data available in the output buffer (even if Data(a) is set to Input mode). In FIFO mode, this port will act as FIFO-Out. If OE(b) is not set, this port will be High-Z.
OE(b)	Input	TBD	**Output Enable.** If set, Data(b) will be set to output-mode, and will reflect output data (in FIFO mode) or Read-Data (in SRAM mode).
OE-INV(b)	Input	TBD	**Output Enable Inverter.** Converts OE(b) to OE(b)#
CS(b)	Input	TBD	**Chip Select (for Port B).** When set, Port-B will respond to commands (such as exporting read data via Data(b) or popping data from the FIFO).
CS-INV(b)	Input	TBD	**Chip Select (for Port B) Inverter.** Converts CS(b) to CS(b)# when set.
CLOCK(b)	Input	TBD	**Sync. Clock (for Port B).** Not used when chip is in Asynchronous mode, but functions as synchronous clock in both Sync FIFO and Sync SRAM modes. Connect to ground when operating in Asynchronous Mode.

PORT B (Continued)			
CLOCK-INV(b)	Input	TBD	**Sync. Clock Inverter.** Once set, in synchronous mode, the chip will respond to falling edges of the clock, instead of rising edge. Not used in Asynchronous mode, and needs to be connected to ground in this scenario.
EMPTY	Output	TBD	**EMPTY.** In FIFO mode, it is used to indicate that no more data is available in the FIFO to be read. Not use in SRAM mode.
EMPTY-INV	Input	TBD	**EMPTY Inverter.** Inverts the 'EMPTY ' pin. Once set, EMPTY pin will be inverted (i.e. 1 = NO MORE DATA TO READ, 0 = DATA AVAILABLE)
GLOBAL			
V(DD)	--	TBD	**Core voltage Supply**. It is recommended to use 10nF bypass capacitors for each V(DD) pin.
V(IO)	--	TBD	**IO Voltage Supply**. A 10nF Bypass capacitor is strongly recommended.
GND	--	TBD	**Ground Supply.**
MODE[0..2]	Input	TBD	**Chip Mode Select .** Functionality of the chip will be determined by the configuration provided through these pins : 000 = Asynchronous SRAM mode 001 = Synchronous SRAM mode 010 = 1-Cycle Latency Sync SRAM mode 011 = 2-Cycle Latency Sync SRAM mode 100 = 3-Cycle Latency Sync SRAM mode 101 = Asynchronous FIFO mode 110 = Sychronous FIFO mode 111 = Reserved (Do Not Use) These pins accept LVCMOS levels
PA-IOT	Input	TBD	**Port-A IO Type.** 1 = LVCMOS, 0 = HSTL. This pin accepts LVCMOS levels Operating speed improves in HSTL mode.
PB-IOT	Input	TBD	**Port-B IO Type.** 1 = LVCMOS, 0 = HSTL. This pin accepts LVCMOS levels Operating speed improves in HSTL mode.
DWSEL[0..1]	Input	TBD	**Data Width Select.** Selects the bit-length of the word in both FIFO and SRAM mode. 00 = 32Bit Words 01 = 24Bit Words 10 = 16Bit Words 11 = 8Bit Words These pins accept LVCMOS levels.

1. Full Asynchronous Mode:



The asynchronous mode has the advantage of being compatible with a wide variety of DSP, Microncontroller and Application-Processor chips, supporting ordinary SRAM memory interface. This model is nearly identical to embedded Block-RAM in FPGAs and requires minimum cost in terms of Logic-Element and LUTs to be implemented on target designs.

It is recommended to HSTL IO standard for FPGA connectivity, as this IO standard provides lower access latency. For high-speed access, general High-Speed PCB layout is recommended. Please check « Appendix. A » for further information.

Figure 1.a – Full Asynchronous Write Operation

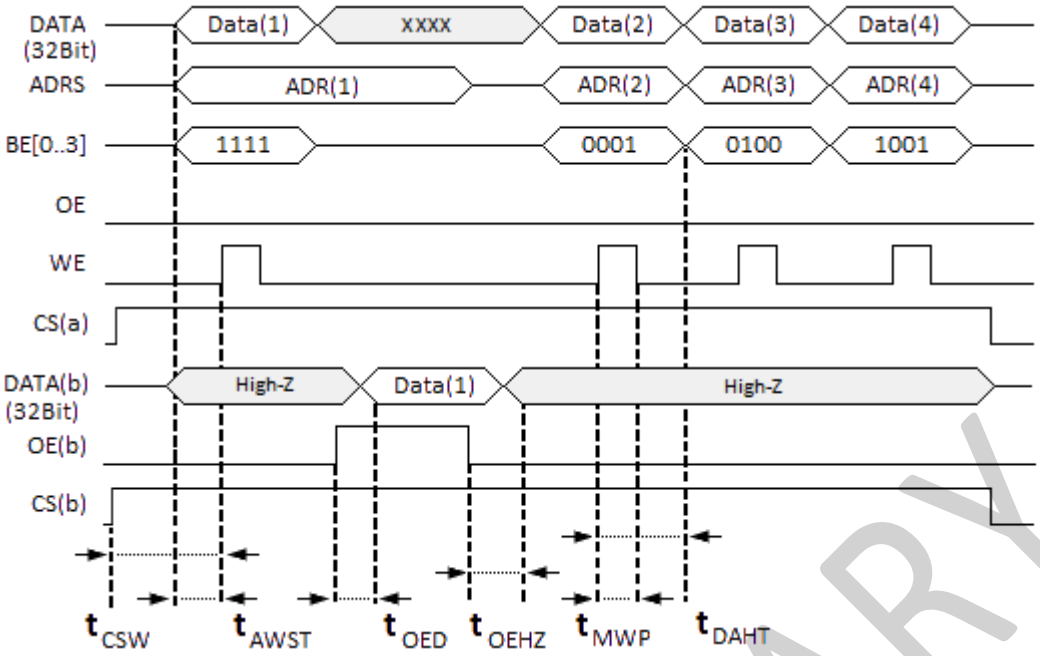
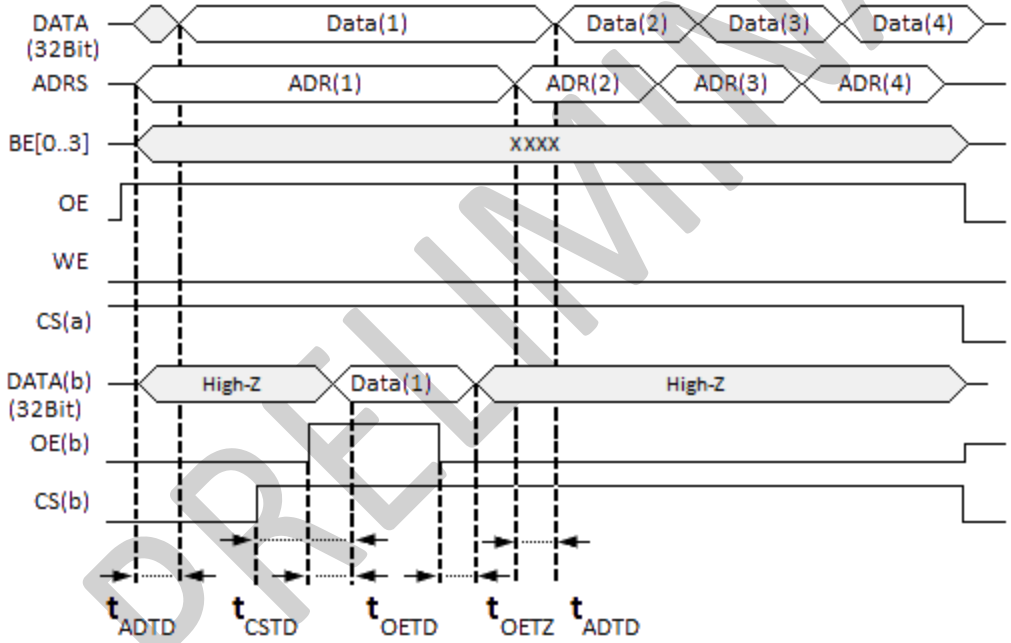


Figure 1.b – Full Asynchronouse Read Operation



Timing and latency characteristics – Asynchronous Mode:

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
Name	**Description**	**Min.**	**Nom.**	**Max.**	**Unit**	**Comments**
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(ADTD)	Address to Data Valid (Read)	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OETZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	

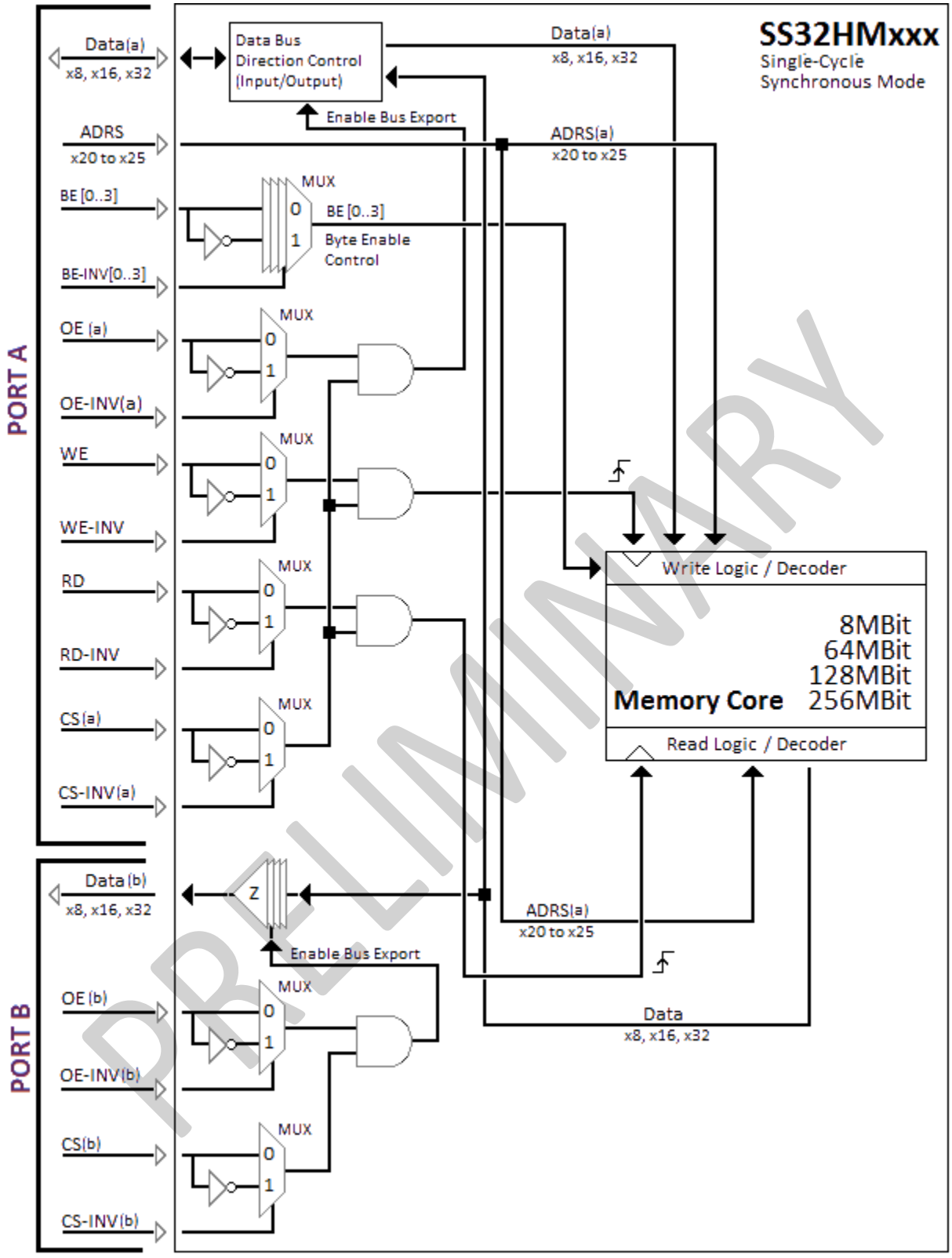
Timing and latency characteristics – Asynchronous Mode (continued)

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
Name	**Description**	**Min.**	**Nom.**	**Max.**	**Unit**	**Comments**
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(ADTD)	Address to Data Valid (Read)	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OETZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(ADTD)	Address to Data Valid (Read)	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OETZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(ADTD)	Address to Data Valid (Read)	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OETZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	

As demonstrated above, the performance increases upon usage of HSTL/SSTL, as LVCMOS requires a higher voltage swing, which in turn, increases the IO Latency. The second port in asynchronous mode acts as an optional read-only port, should the user choose not to use the Port-A for both read and write purposes.

To further optimize the performance, the « Single-Cycle Synchronous » mode could be used. It essentially is the same as asynchronous in write-mode and differs only in reading, as an « RD » strobe is required to read from the memory.

2. Single-Cycle Sychronous Mode :



The structure of Single-Cycle Synchronous mode is similar to Full-Asynchronous, with the sole exception of “RD” pin being used to execute a memory-read (RD acts as Read-Strobe). Once the chip receives an “RD” pulse, it will provide the data at the output pins within a fixed period of time, known as “$t_{(RDDV)}$”.

The “Write” operation is identical to Full-Async mode, and only “Read” operation differs, as an “RD” strobe is required to read data from the memory.

Figure 2.a – Single-Cycle Synchronous Write Operation

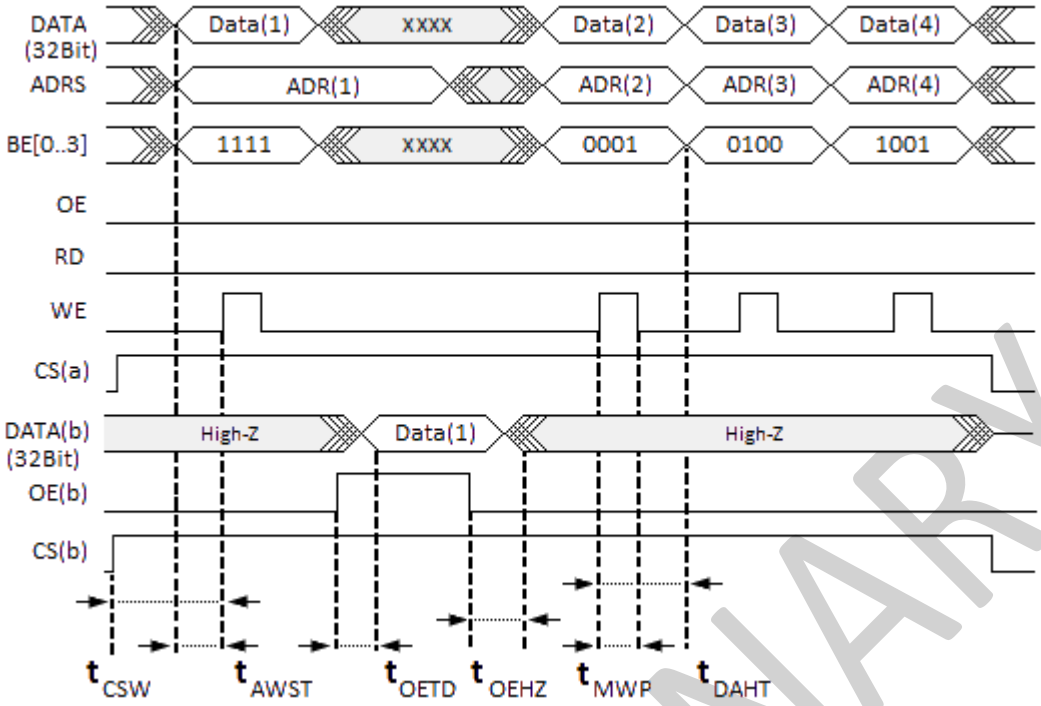
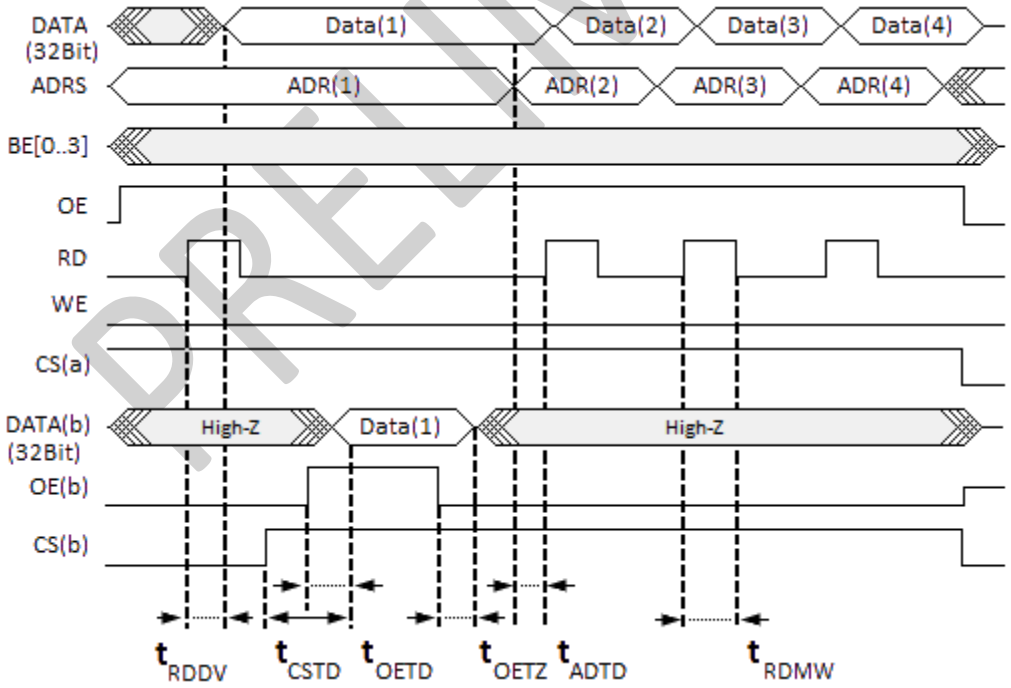


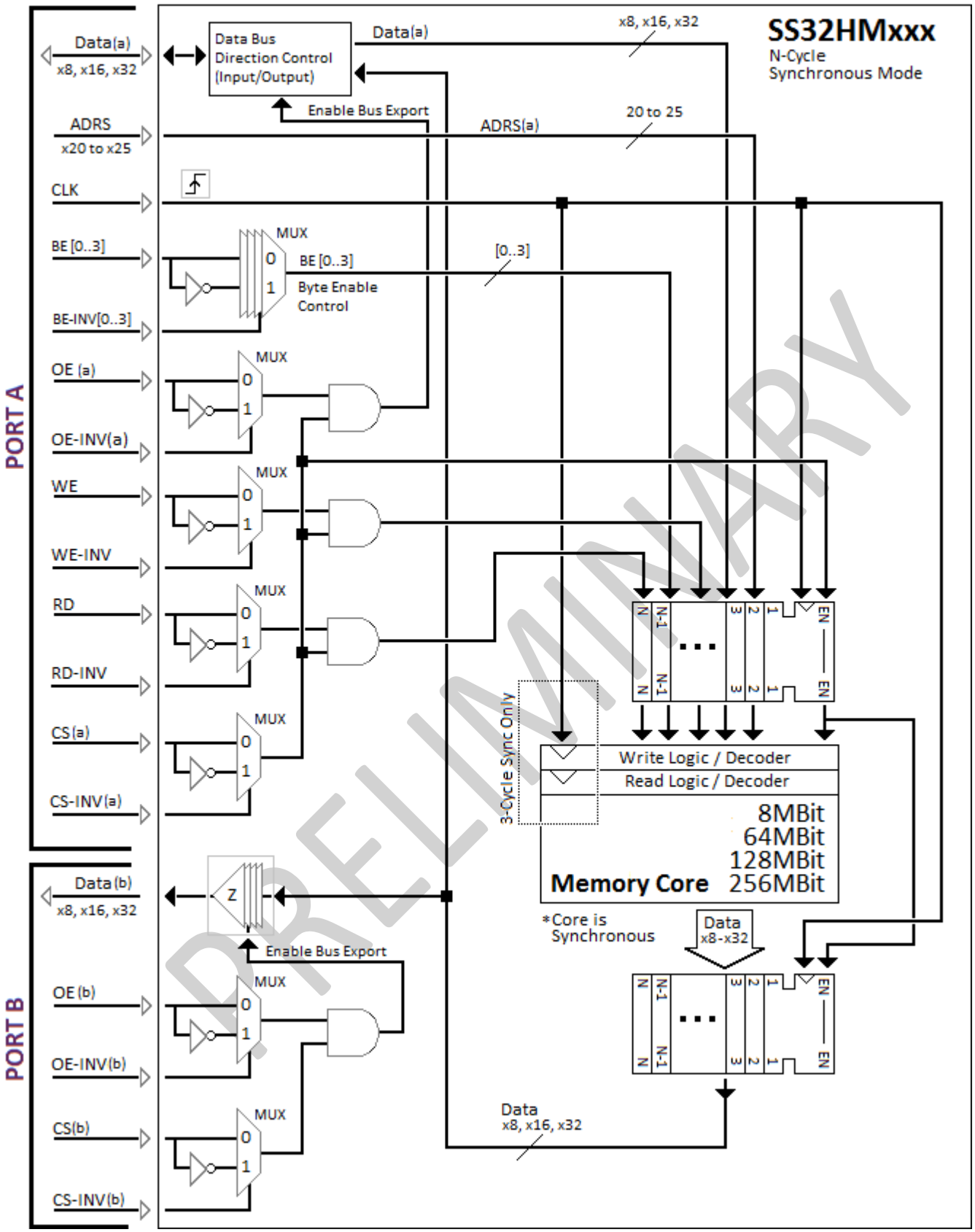
Figure 2.b – Single-Cycle Synchronous Read Operation



Timing and latency characteristics – Single-Cycle Sync Mode:

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
Name	**Description**	**Min.**	**Nom.**	**Max.**	**Unit**	**Comments**
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST) t(ADTD)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(RDDV)	Read-Strobe to Data Valid (Read)	TBD	TBD	TBD	ns	
t(RDMW)	Read-Strobe Minimum Pulse Width	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OEHZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	
Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST) t(ADTD)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(RDDV)	Read-Strobe to Data Valid (Read)	TBD	TBD	TBD	ns	
t(RDMW)	Read-Strobe Minimum Pulse Width	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OEHZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST) t(ADTD)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(RDDV)	Read-Strobe to Data Valid (Read)	TBD	TBD	TBD	ns	
t(RDMW)	Read-Strobe Minimum Pulse Width	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OEHZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSW)	CS to Write	TBD	TBD	TBD	ns	
t(AWST) t(ADTD)	Setup-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(MWP)	Minimum Write Pulse Width	TBD	TBD	TBD	ns	
t(DAHT)	Hold-Time for Data, Address and BE	TBD	TBD	TBD	ns	
t(RDDV)	Read-Strobe to Data Valid (Read)	TBD	TBD	TBD	ns	
t(RDMW)	Read-Strobe Minimum Pulse Width	TBD	TBD	TBD	ns	
t(CSTD)	CS to Data-Valid	TBD	TBD	TBD	ns	
t(OETD)	OE to Data-Valid (Tri-State Buffer Latency)	TBD	TBD	TBD	ns	
t(OEHZ)	Wait-Time after OE until Bus becomes Hi-Z	TBD	TBD	TBD	ns	

3. N-Cycle Sychronous Mode :



In the N-Cycle synchronous mode, either two or three cycles are required for read and write operation. Being pipelined allows the chip to receive read/write commands without interruption. The advantage of three-cycle synchronous mode over two-cycle synchronous mode is the maximum operating clock-speed (with 3-Cycle being faster).

Figure 3.a – N-Cycle Synchronous Write Operation

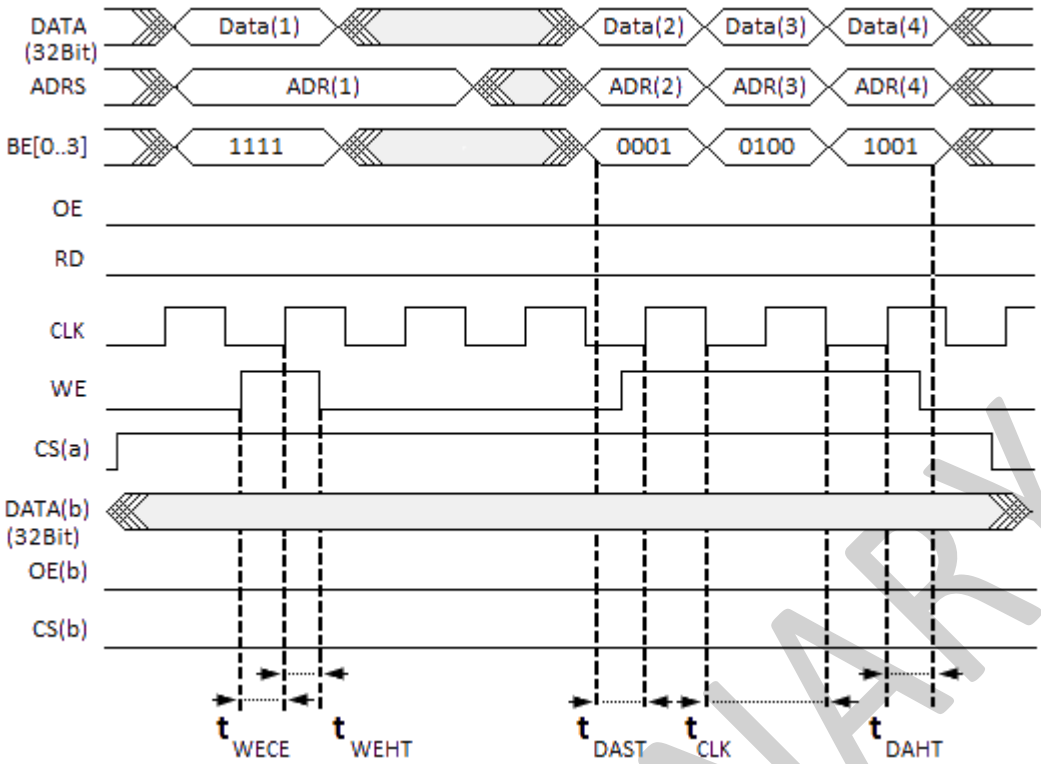
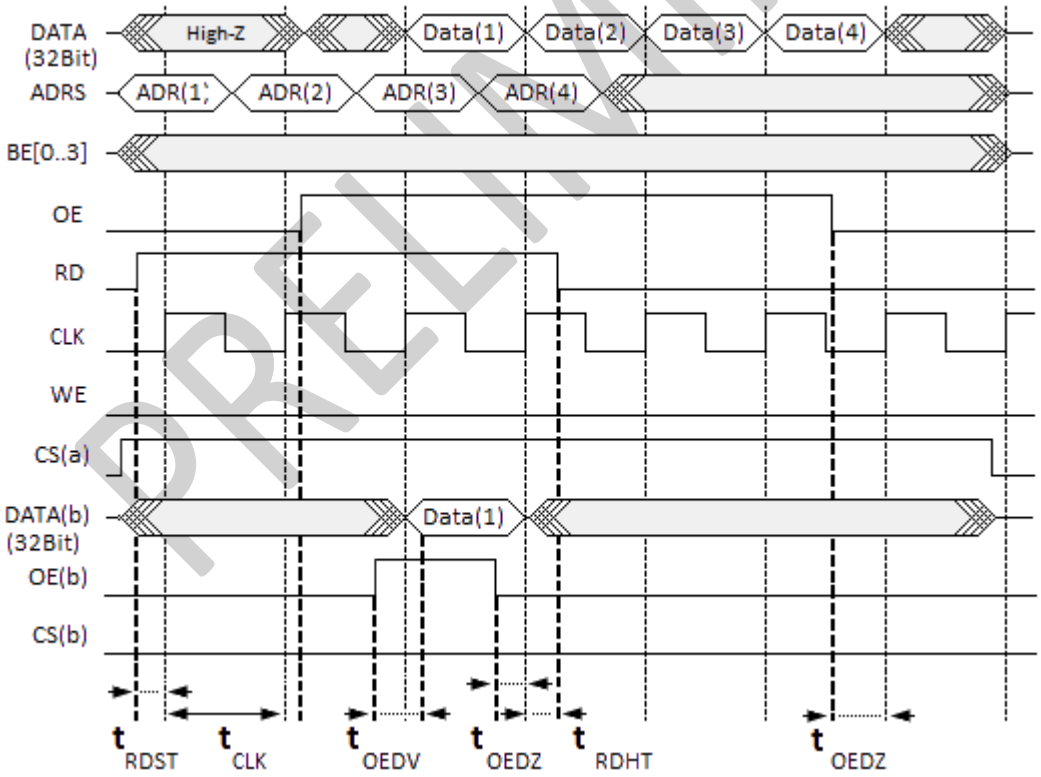


Figure 3.b – N-Cycle Synchronous Read Operation



Note: The waveform above demonstrates a 2-Cycle latency operation, meaning that the chip will provide data on the output bus (in a Read-Operation), at the 3rd rising clock-edge following a read command. The 3-Cycle operation is identical; with the exception of data being available at the 4th rising edge of the clock following a read-command is issued. These operations are fully pipelined.

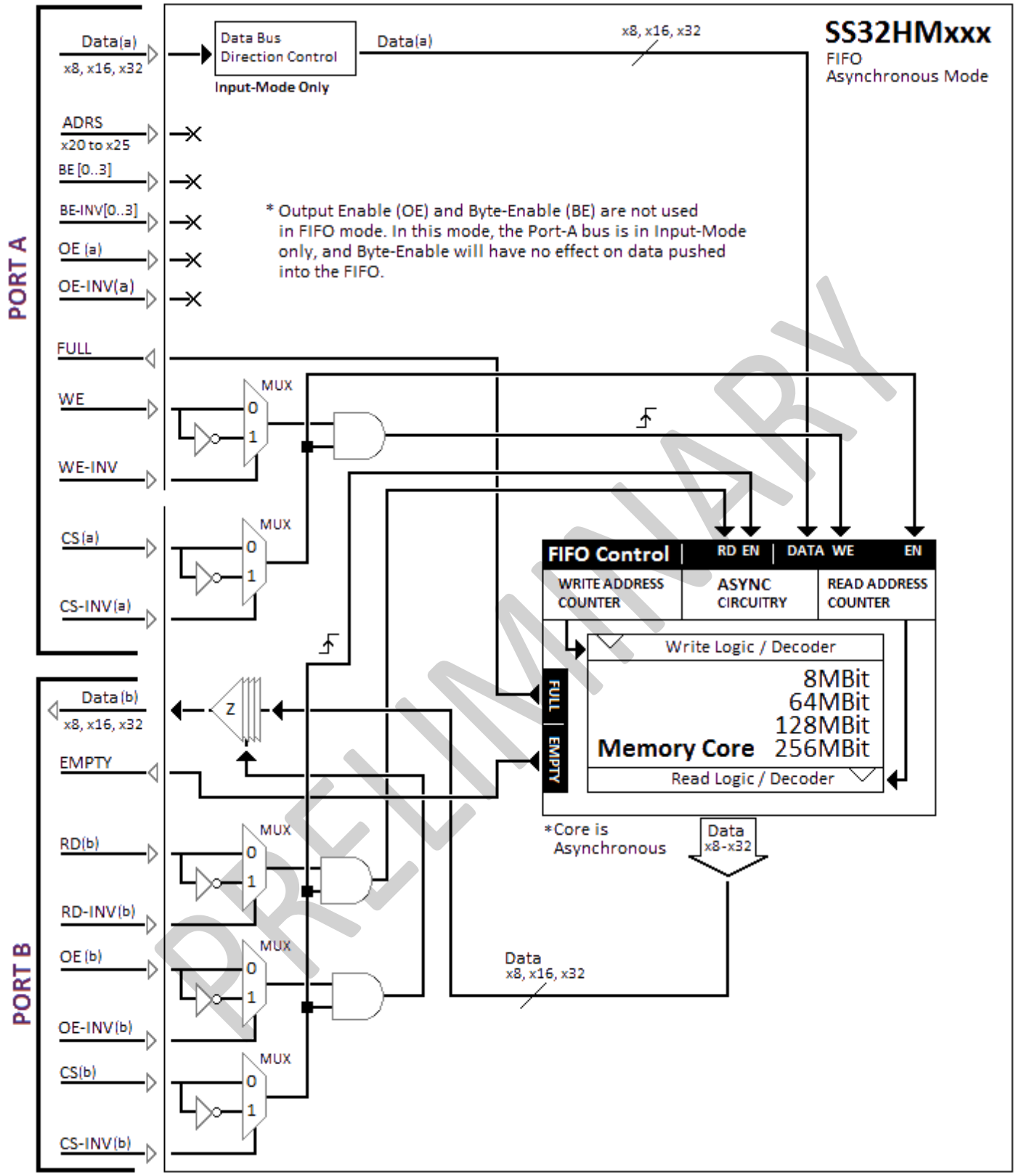
Timing and latency characteristics – N-Cycle Sync Mode (2-Cycle Latency):

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
Name	**Description**	**Min.**	**Nom.**	**Max.**	**Unit**	**Comments**
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	
Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	

Timing and latency characteristics – N-Cycle Sync Mode (3-Cycle Latency):

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
Name	**Description**	**Min.**	**Nom.**	**Max.**	**Unit**	**Comments**
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	
Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSCE)	Minimum CS activate Before Clock Edge	TBD	TBD	TBD	ns	
t(WECE)	Write-Enable to Clock-Edge	TBD	TBD	TBD	ns	
t(WEHT)	Write-Enable Hold Time After Clock	TBD	TBD	TBD	ns	
t(DAST)	Data/Address/BE Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(DAHT)	Data/Address/BE Hold-Time After Clock	TBD	TBD	TBD	ns	
t(RDST)	Read Setup-Time Before Clock	TBD	TBD	TBD	ns	
t(RDHT)	Read Hold-Time After Clock	TBD	TBD	TBD	ns	
t(OEDV)	Output-Enable activate to Data Valid	TBD	TBD	TBD	ns	
t(OEDZ)	Output-Enable deactivate to Data High-Z	TBD	TBD	TBD	ns	
t(CLK)	Clock Frequency (Duty-Cycle) : 50%	TBD	TBD	TBD	ns	

4. Asynchronous FIFO Mode :



Asynchronous FIFO mode uses Write-Enable (WE) pin as strobe for pushing data in, and Read-Enable (RD) pin as strong for popping data out. This mode is slower than Sync FIFO, and requires no Clock.

Figure 4.a – Pushing data in the Asynchronous FIFO :

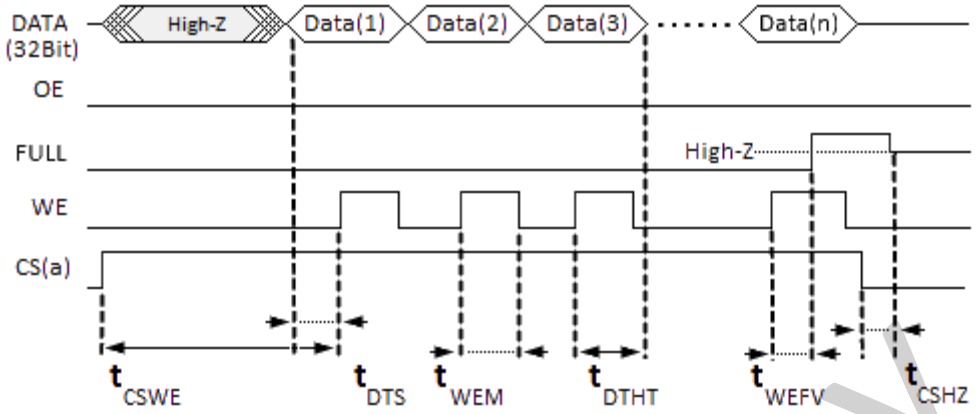
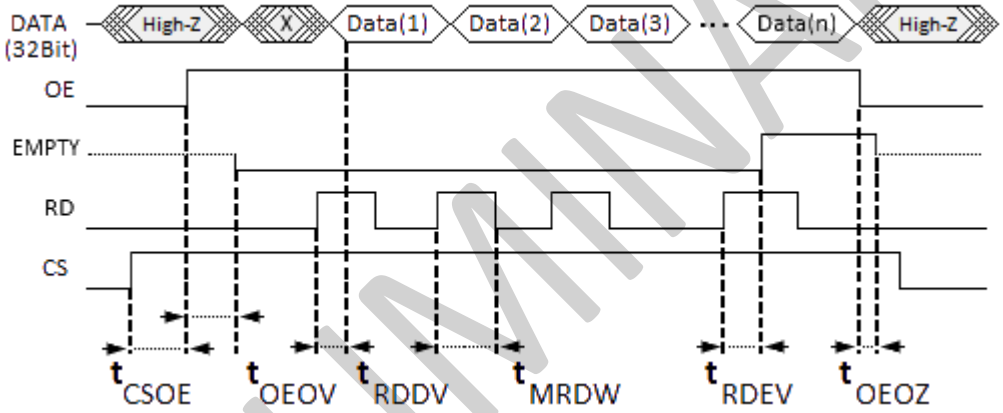


Figure 4.b – Popping data from the Asynchronous FIFO :

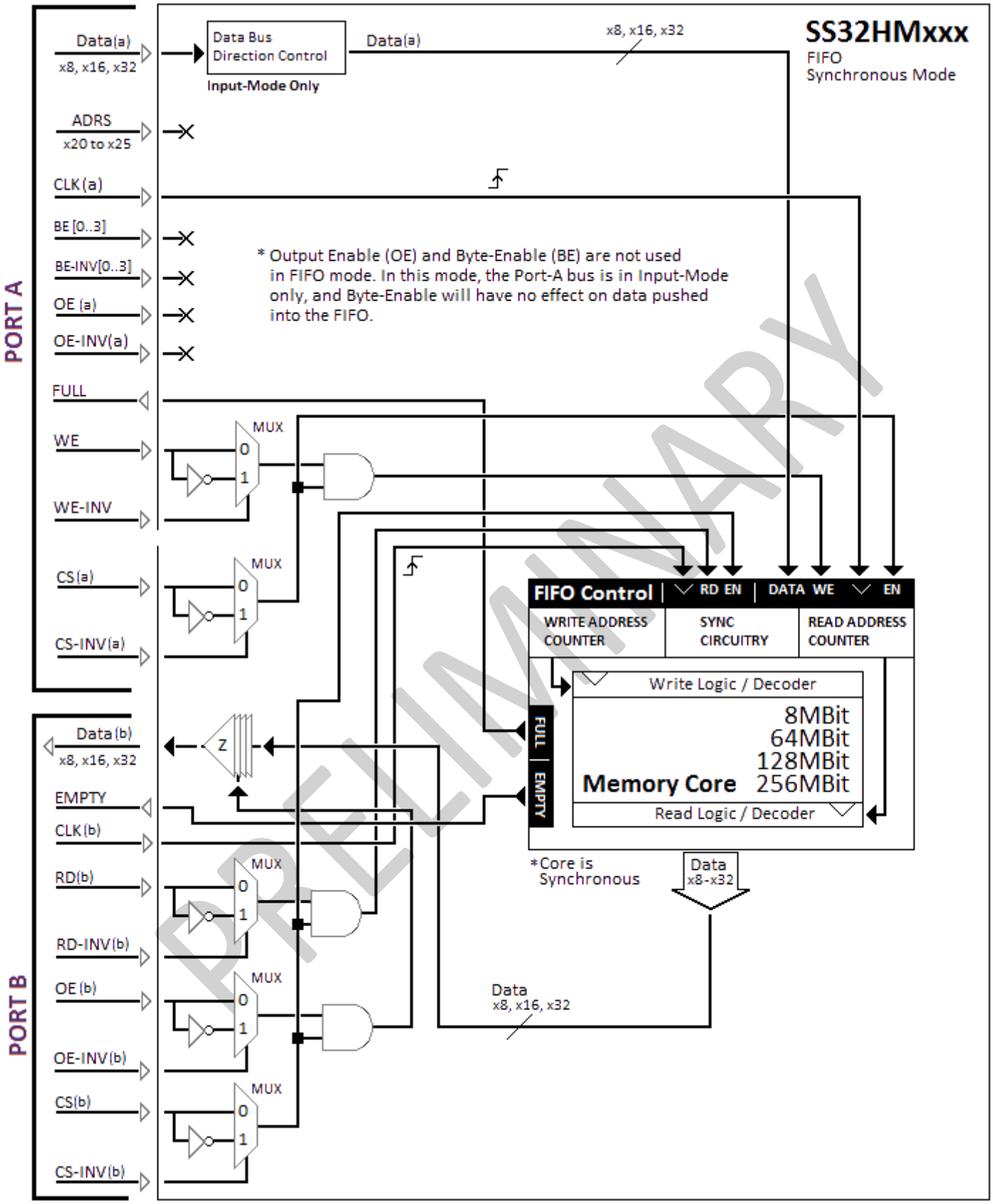


Timing and latency characteristics – Async FIFO Mode:

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
Name	**Description**	**Min.**	**Nom.**	**Max.**	**Unit**	**Comments**
t(CSWE)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(DTS)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(WEM)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(DTHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(WEFV)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(CSHZ)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(CSOE)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(OEOV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDDV)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	
t(MRDW)	Minimum RD pulse needed	TBD	TBD	TBD	ns	
t(RDEV)	RD rising-edge to EMPTY pin valid	TBD	TBD	TBD	ns	
t(OEOZ)	OE deactivate to Data/EMPTY going High-Z	TBD	TBD	TBD	ns	

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSWE)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(DTS)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(WEM)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(DTHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(WEFV)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(CSHZ)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(CSOE)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(OEOV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDDV)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	
t(MRDW)	Minimum RD pulse needed	TBD	TBD	TBD	ns	
t(RDEV)	RD rising-edge to EMPTY pin valid	TBD	TBD	TBD	ns	
t(OEOZ)	OE deactivate to Data/EMPTY going High-Z	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
t(CSWE)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(DTS)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(WEM)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(DTHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(WEFV)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(CSHZ)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(CSOE)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(OEOV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDDV)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	
t(MRDW)	Minimum RD pulse needed	TBD	TBD	TBD	ns	
t(RDEV)	RD rising-edge to EMPTY pin valid	TBD	TBD	TBD	ns	
t(OEOZ)	OE deactivate to Data/EMPTY going High-Z	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(CSWE)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(DTS)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(WEM)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(DTHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(WEFV)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(CSHZ)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(CSOE)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(OEOV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDDV)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	
t(MRDW)	Minimum RD pulse needed	TBD	TBD	TBD	ns	
t(RDEV)	RD rising-edge to EMPTY pin valid	TBD	TBD	TBD	ns	
t(OEOZ)	OE deactivate to Data/EMPTY going High-Z	TBD	TBD	TBD	ns	

5. Synchronous FIFO Mode :



Achievable clock speed in Sync FIFO is higher than Async FIFO. However, there will be a few clock latencies (due to pipelining) for input data to propagate. The chip can accept different Write and Read clocks in this mode, making it suitable for crossing clock domains.

Figure 5.a – Pushing data in the Synchrounous FIFO :

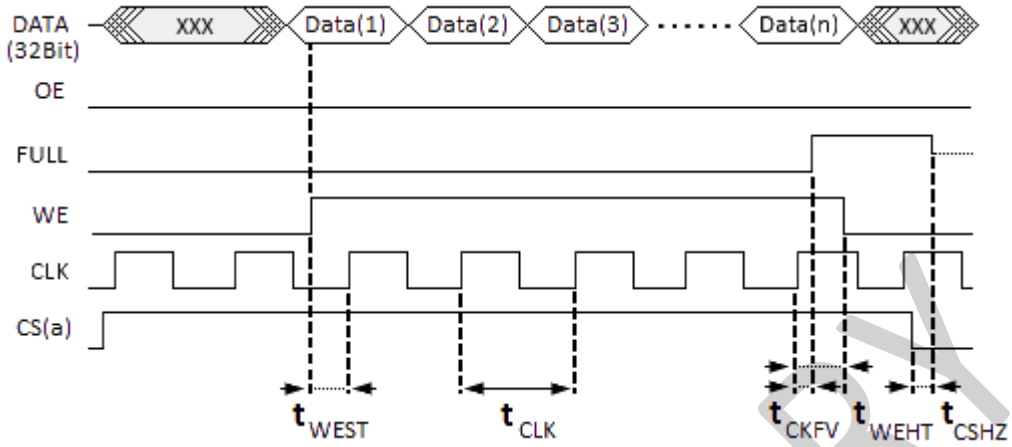
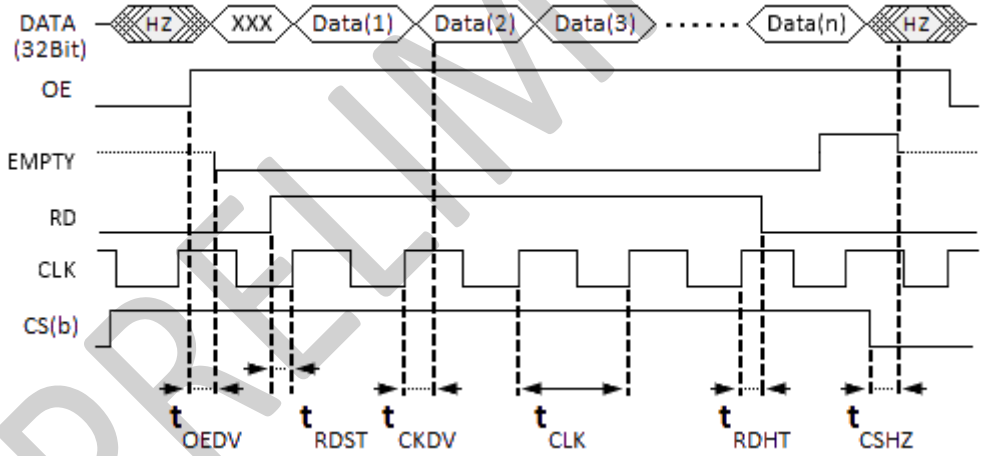


Figure 5.b – Popping data from the Synchronous FIFO :



The synchronous FIFO can operate at much higher clock rates due to internal pipelined architecture. This enables it to be used as data buffer in situations where two domains operate at different clock speeds (Fiber communication, high-speed Analog-To-Digital or Digital-To-Analog conversion, Direct Digital Synthesis, etc.).

Timing and latency characteristics – Sync FIFO Mode:

Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
Name	**Description**	**Min.**	**Nom.**	**Max.**	**Unit**	**Comments**
t(WEST)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(CLK)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(CKFV)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(WEHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(CSHZ)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(OEDV)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(RDST)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(CKDV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDHT)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	
Vdd = 3.3V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(WEST)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(CLK)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(CKFV)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(WEHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(CSHZ)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(OEDV)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(RDST)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(CKDV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDHT)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = HSTL/SSTL						
t(WEST)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(CLK)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(CKFV)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(WEHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(CSHZ)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(OEDV)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(RDST)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(CKDV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDHT)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	
Vdd = 1.8V, Temp = -10°C, 25°C, 85°C, I/O = LVCMOS						
t(WEST)	Minimum CS wait before a WE is issued	TBD	TBD	TBD	ns	
t(CLK)	Data Setup Time (before WE is issued)	TBD	TBD	TBD	ns	
t(CKFV)	Minimum pulse duration required for WE	TBD	TBD	TBD	ns	
t(WEHT)	Data Hold Time (after WE edge)	TBD	TBD	TBD	ns	
t(CSHZ)	Latency after WE to have a valid 'FULL'	TBD	TBD	TBD	ns	
t(OEDV)	CS deactivate to outputs going High-Z	TBD	TBD	TBD	ns	
t(RDST)	CS activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(CKDV)	OE activate to Data/EMPTY valid	TBD	TBD	TBD	ns	
t(RDHT)	Latency after RD to have valid Data	TBD	TBD	TBD	ns	